AND8152/D

Using the NCP5331 2-Phase Controller for NVIDIA Video Card Applications (NV38)

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APPLICATION NOTE

1. What is the maximum PWM frequency the NCP5331 can operate without overheating, due to the internal gate driver power dissipation?

- To minimize the cost and PCB area, assume we are using one upper and one lower FET. Both FETs are in the DPAK package.
- This depends on the Vgs voltage, FET gate charge to Vgs, and the number of upper and lower FETs used.
- Upper FET: Choose the NTD60N02 because of its low gate charge. If VCCH = 12 V, then the gate drive pins will be approximately 11 V.

5.0 V Phase: V_{GS} = 11 V−5.0 V = 6.0 V_{GS}
3.3 V Phase: V_{GS} = 11 V−3.3 V = 7.7 V_{GS}

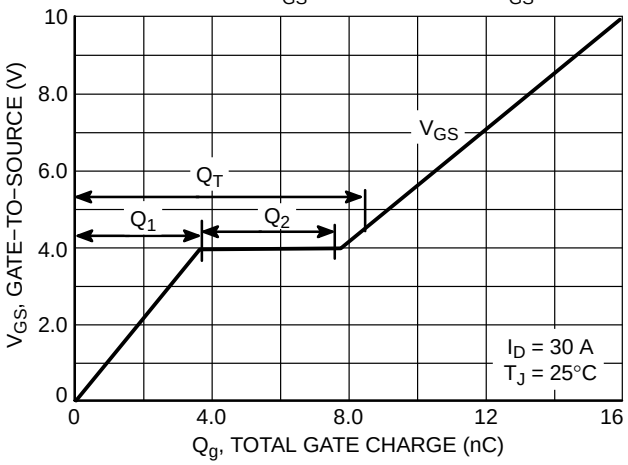


Figure 1. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

Qg @ 6.0 V_{GS} = 10.3 nC
Qg @ 7.7 V_{GS} = 12.9 nC

- Lower FET: Choose the NTD110N02 because of its low RDSon and its low ratio of Qgd/Qgs1. Qgd is the gate to drain charge and Qgs1 is the pre−turn−on threshold gate to source charge (see PCIM May 2000 publication). A low ratio indicates a good synchronous FET because it will resist dv/dt turn−on via the switch node.

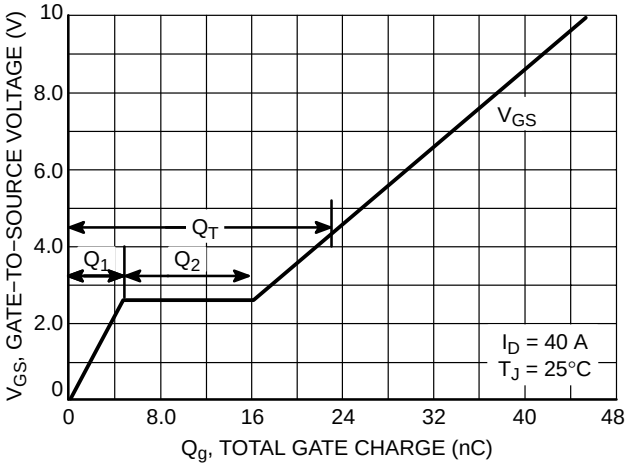


Figure 2.

Qgd/Qgs1 = (16 nC−5.0 nC)/3.0 nC = 3.6:1
Qg @ 10 V = 46 nC

- What is the maximum power dissipation of the LQFP−32 package for a particular PCB temperature?
  Tj_max = 125°C
  Tpcb = 80°C (this is the assumed PCB temperature with minimal airflow)
  $R_{\theta ja}$ = 52°C/W (from our data sheet dated June 2003)

  (125°C–80°C)/(52°C/W) = 0.865 W maximum *total* power dissipation
- The DC losses in the NCP5331:
  = Losses at V_{CC} + Losses at V_{CCH} + Losses at V_{CCL1} and V_{CCL2}
  = 12 V*22 mA + 12 V*6.4 mA + 2.0*12 V*5.0 mA
  = 0.461 W due to the quiescent currents
- The losses available for switching without overheating the controller:
  0.865 W–0.461 W = 0.404 W

- Add all the switching losses and equate them to the losses available for switching:

  = Upper FET losses at 6.0 V + Upper FET losses at 7.7 V + 2.0*Lower FET losses at 12 V
  = 10.3 nC*6.0 V*fsw + 12.9 nC*7.7 V*fsw + 2.0*10 V*46 nC*fsw
  = 0.404 W

  Solving for fsw results in 374 kHz for a maximum switching frequency with these FETs.

  Select a PWM operating frequency less than this maximum – 225 kHz.

- Check the minimum pulse width at 225 kHz with the minimum output voltage (0.8 V) and maximum input voltage (13.2 V) at the maximum frequency (+20%):
  ton = 0.8 V/5.5 V/(1.2*225 kHz) = 538.7 ns
  This is much higher than the worst case minimum pulse width of 280 ns specified in the NCP5331 data sheet. If the switching frequency were set too high then the minimum pulse width would become very important. Too high of a switching frequency would result in pulse skipping (voltage jitter) at the lowest VID settings and/or highest input voltages.

2. What is the power being dissipated by the FETs?

- Assume the total output current from the 2−phase converter is 30 A maximum. Based on NVIDIA's choice of FETS in the reference design (12 A max continuous rating), the actual current requirement should be less − this should be a conservative design. Also, choose a nominal output voltage such as 1.2 V to do the design.
- Assume the 2−phases must be balanced to maximize the available power without violating current limitations of the AGP pin. The reference design from NVIDIA appears to draw 1.5 x more current from the 5.0 V phase than from the 3.3 V phase. However, conversion from the 5.0 V phase at 1.5 x the current will certainly be less efficient than conversion from the 3.3 V phase at 1.0 x the current. Using an efficiency of 80% for the 5.0 V phase and 90% from the 3.3 V phase we will distribute the currents to account for the differences in efficiency.
  Efficiencies: I_5.0 V/I_3.3 V = [80% x 5.0 V]/[90% x 3.3 V]
  Currents: I_5.0 V + I_3.3 V = 30 A
  Solve the first equation for I_5.0 V and substitute into the second equation:
  1.34 x I_3.3 V + I_3.3 V = 30 A then
  I_3.3 V = 12.8 A and
  I_5.0 V = 30 A–12.8 A = 17.2 A
- Calculate the power dissipated by the upper mosfet. Losses in the upper mosfet will be dominated by the switching losses and, depending on R_{DSon} and the duty−cycle, the conduction losses. Neglect secondary losses due to the upper and lower mosfet output charge (Qoss) and the reverse recovery time (trr) of the lower mosfet.
  Igate = gate driver output current of the NCP5331 = 1.0 A
  Qswitch = the post gate threshold charge plus the gate to source charge of the 60N02 = 6.5 nC

5.0 V Phase − Upper MosFET R_{DSon} of 60N02 @ 6.0 V_{gs}, T_j = 125°C = 14.9 mΩ	**3.3 V Phase − Upper MosFET** R_{DSon} of 60N02 @ 7.7 V_{gs}, T_j = 125°C = 13.7 mΩ
$\Delta I_L = \Delta V/L * \Delta t$ = (5.0 V−1.2 V)/875 nH * (1.2 V/5.0 V)/225 kHz = 4.63 A peak−to−peak (A_{PP})	$\Delta I_L = \Delta V/L * \Delta t$ = (3.3 V−1.2 V)/875 nH * (1.2 V/3.3 V)/225 kHz = 3.88 A peak−to−peak (A_{PP})
$Irms = [D * 17.2\ A^2]^{1/2}$ $= [(1.2\ V/5.0\ V) * 295.8]^{1/2}$ = 8.42 Arms	$Irms = [D * 12.8\ A^2]^{1/2}$ $= [(1.2\ V/3.3\ V) * 163.8]^{1/2}$ = 7.72 Arms
$Pd = Irms^2*R_{DSon} + Io\_peak*t_{switch}*V_{in}*fsw$ $= Irms^2*R_{DSon} + (Io\_avg + \Delta Io/2)$ $*(Qswitch/Igate)*V_{in}*fsw$ $= 8.42^2$ Arms*14.9 mΩ + (17.2 A + 4.63 A_{PP}/2) *(6.5 nC/1.0 A)*5.0 V*225 kHz = 1.06 W + 0.14 W = 1.20 W	$Pd = Irms^2*R_{DSon} + Io\_peak*t_{switch}*V_{in}*fsw$ $= Irms^2*R_{DSon} + (Io\_avg + \Delta Io/2)$ $*(Qswitch/Igate)*V_{in}*fsw$ $= 7.72^2$ Arms*13.7 mΩ + (12.8 A + 3.88 A_{PP}/2) *(6.5 nC/1.0 A)*3.3 V*225 kHz = 0.82 W + 0.071 W = 0.89 W

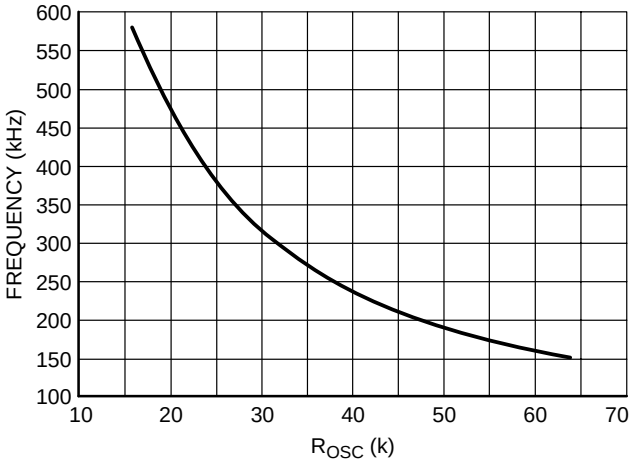
- The exact thermal solution is left to the customer. To derive an effective heatsink design, each application must consider airflow, mechanical requirements, case operating temperature goals, PCB and ambient operating temperatures, and cost.
- Calculate the power dissipated by the lower mosfets. Losses in the lower mosfets are dominated by the conduction losses and the diode losses during non−overlap time.

5.0 V Phase − Lower MosFET R_{DSon} of 110N02 @ 10 V_{gs}, T_j = 125°C = 6.0 mΩ T_nonoverlap = 65 ns for the NCP5331 gate drivers Vf = diode voltage of the 110N02 @ 15 A = 0.78 V	**3.3 V Phase − Lower MosFET** R_{DSon} of 110N02 @ 10 V_{gs}, T_j = 125°C = 6.0 mΩ T_nonoverlap = 65 ns for the NCP5331 gate drivers Vf = diode voltage of the 110N02 @ 15 A = 0.78 V
Irms = $[(1.0-D) * 17.2\ A^2]^{1/2}$ = $[(1.0-1.2\ V/5.0\ V) * 295.8]^{1/2}$ = 14.99 Arms	Irms = $[(1.0-D) * 12.8\ A^2]^{1/2}$ = $[(1.0-1.2\ V/3.3\ V) * 163.8]^{1/2}$ = 10.2 Arms
Pd = $Irms^2 * R_{DSon}$ + Vf*Io*t_nonoverlap*fsw = 14.99^2 A*6.0 mΩ + 0.78 V*17.2 A*65 ns*225 kHz = 1.35 W + 0.196 W = 1.55 W	Pd = $Irms^2 * R_{DSon}$ + Vf*Io*t_nonoverlap*fsw = 10.2^2 A*6.0 mΩ + 0.78 V*12.8 A*65 ns*225 kHz = 0.624 W + 0.146 W = 0.770 W

- The exact thermal solution is left to the customer. To derive an effective heatsink design, each application must consider airflow, mechanical requirements, case operating temperature goals, PCB and ambient operating temperatures, and cost.

3. Determine the passive components around the NCP5331.

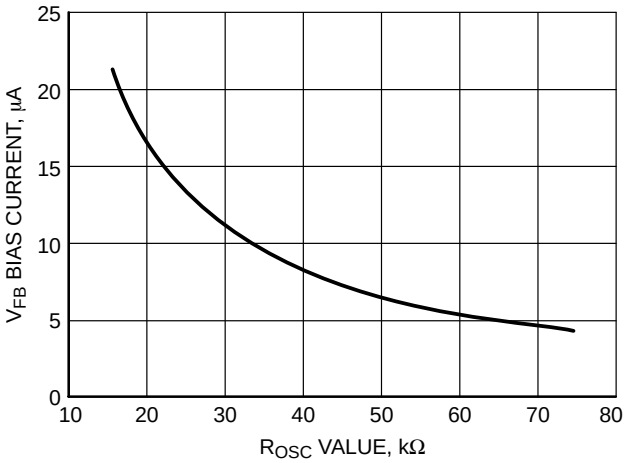
- Assume the NV38 video card application has the following requirements:
  - Output voltage range: 0.8 V–1.5 V
  - Maximum output current: 30 A
  - Output Inductors are 750 nH–1.0 μH (use 875 nH average), 2.5 mΩ
  - Switching frequency (fsw) = 225 kHz (derived on pages 1 and 2 of this paper)
  - Voltage droop due to Adaptive Voltage Positioning (AVP) at full−load shall be 0 V
  - No−Load offset voltage (AVP) above the DAC shall be ≤ 0.2% at any DAC setting
- First, determine the value of Rosc to set the switching frequency to 225 kHz by using Figure 3 from the NCP5331 data sheet:



R_{osc} = 42.2 K to obtain 225 kHz

Figure 3. Oscillator Frequency vs. R_{OSC} Value

- Next, we must choose a value of the feedback resistor, RFB. Before calculating a value, we must know the feedback bias current. The feedback bias current can be found from Figure 4 from the NCP5331 data sheet once the value of Rosc (42.2 K) is known:



IFB = 7.5 μA @ R_{osc} = 42.2 K

Figure 4. V_{FB} Current vs. R_{OSC} Value

In a typical multi−phase CPU application, IFB and the value of RFB determine the No−Load AVP voltage above the DAC setting. For the graphic card application, we want minimal no−load deviation above the DAC (<0.2% of the DAC setting). This will be accomplished by applying an external bias current via a resistor (Rbias) from the 5.0 V Reference output (pin 8) to VFB (pin 1) as shown in the application schematic. The value of this bias resistor can be calculated with the following equation:

Rbias = (Vref–DAC)/IFB
= (5.0 V–1.2 V)/7.5 μA
= 506.6 K (511 K is a standard value)

Adding this bias current allows more flexibility in choosing the value of RFB and provides better transient response. Without the bias current, RFB would need to be very low (<<1.0 K) to minimize the no−load AVP setting. A low value of RFB is not desirable because load transients

will demand more current from the error amplifier to maintain closed loop operation. If RFB is too low, the error amplifier will current limit during output transients and the error amplifier will not be able to maintain control of the VFB node (i.e. the error amplifier will be open loop and the output voltage unregulated). A value of at least 1.0 K is recommended for RFB – we will choose 2.0 K for this application.

The value of Rbias is optimized when the DAC is set to 1.2 V (the nominal design point). At other DAC settings the external bias current will change and add error to the output voltage. The following table shows that this additional error is less than 0.2% at the minimum and maximum DAC settings.

Table 1.

DAC Setting (V)	Ext. Bias w/511 K (μA)	Output Error w/RFB = 2.0 K (mV)	Percent Error
0.80	8.21	−1.40	0.175%
1.20	7.43	+0.14	0.012%
1.50	6.85	+1.30	0.087%

- To set ZERO droop at full−load, the “droop resistor” from VDRP to VFB must be unpopulated.

- Determine the Error Amplifier Compensation components: A good compensation scheme must provide robust stability and acceptable transient response. The following graphs demonstrate the stability by documenting the transient response and the bode plot. The transient response shows no instability or ringing. The bode plot indicates the system will have 9.8 kHz of bandwidth, 129 degrees of phase margin, and at least 30 dB of gain margin.

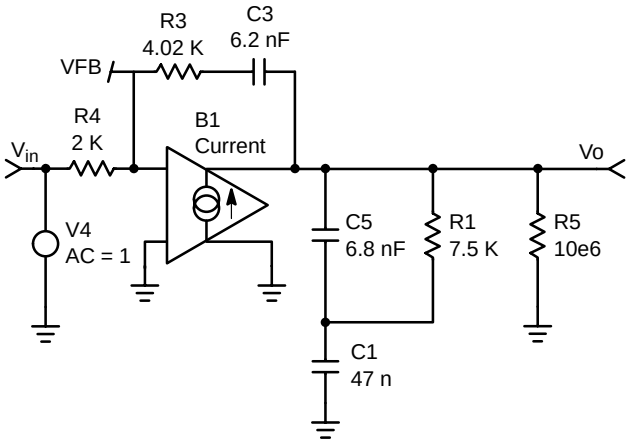


Figure 5. NCP5331 Error Amplifier Compensation

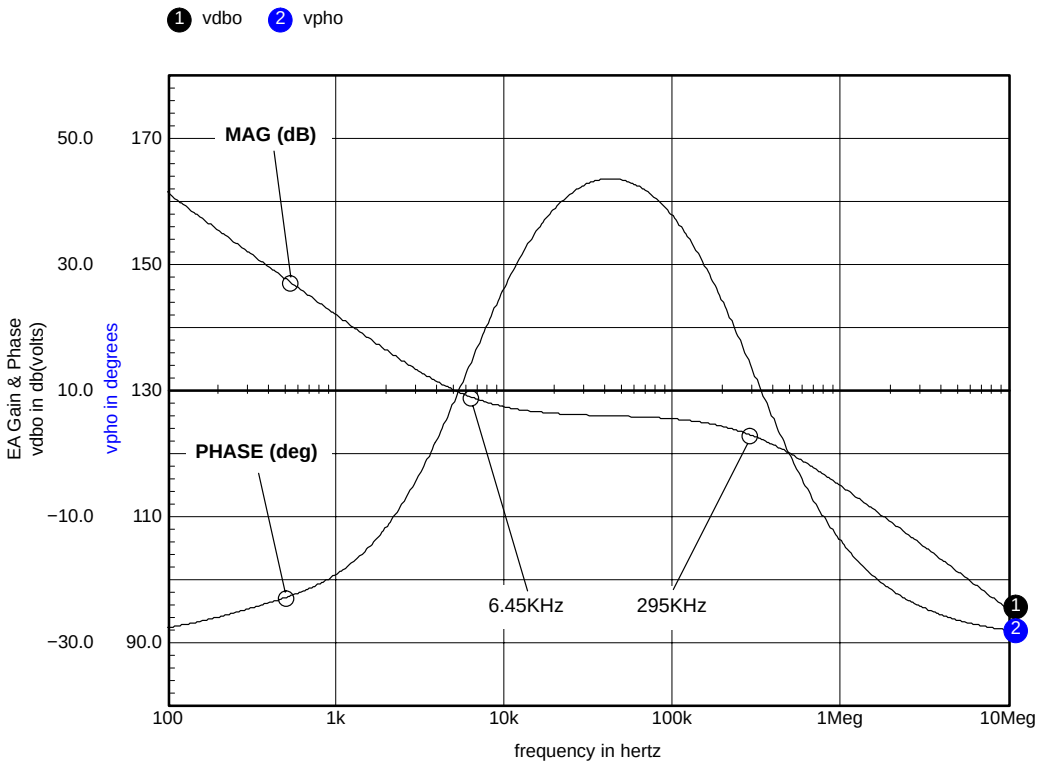


Figure 6. Error Amplifier Gain and Phase Plots

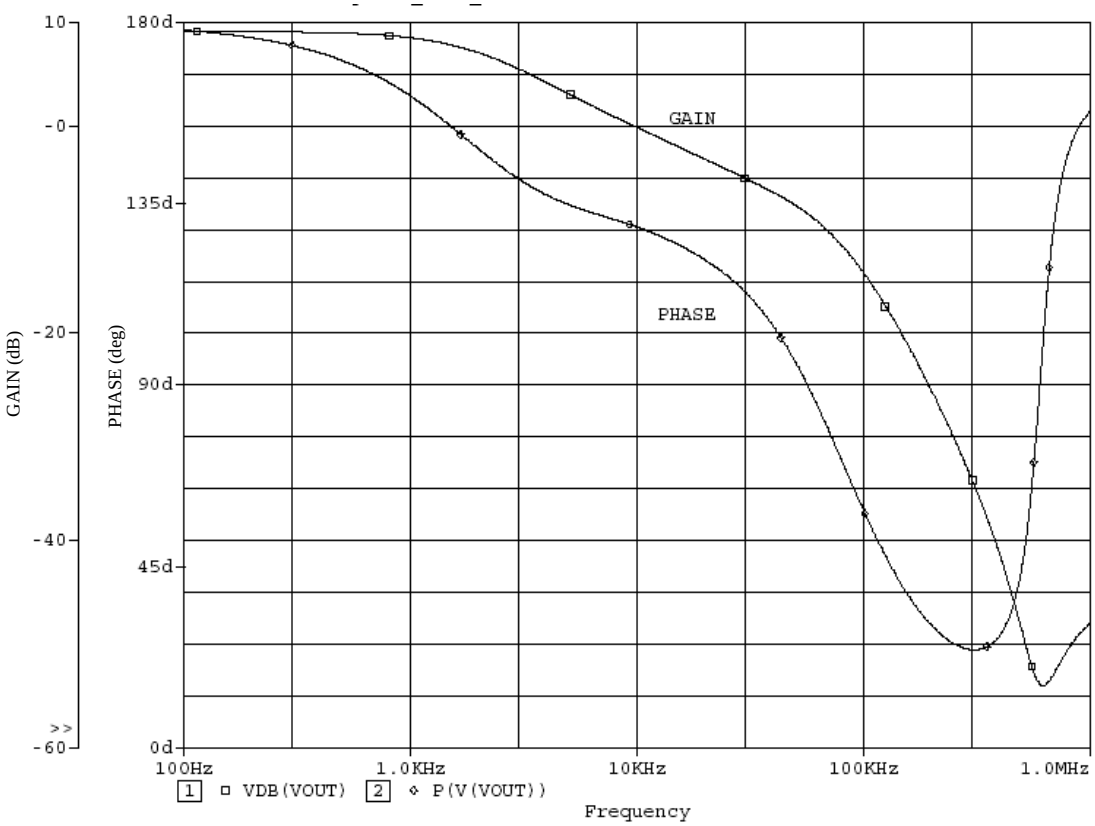


Figure 7. System Bode Plot

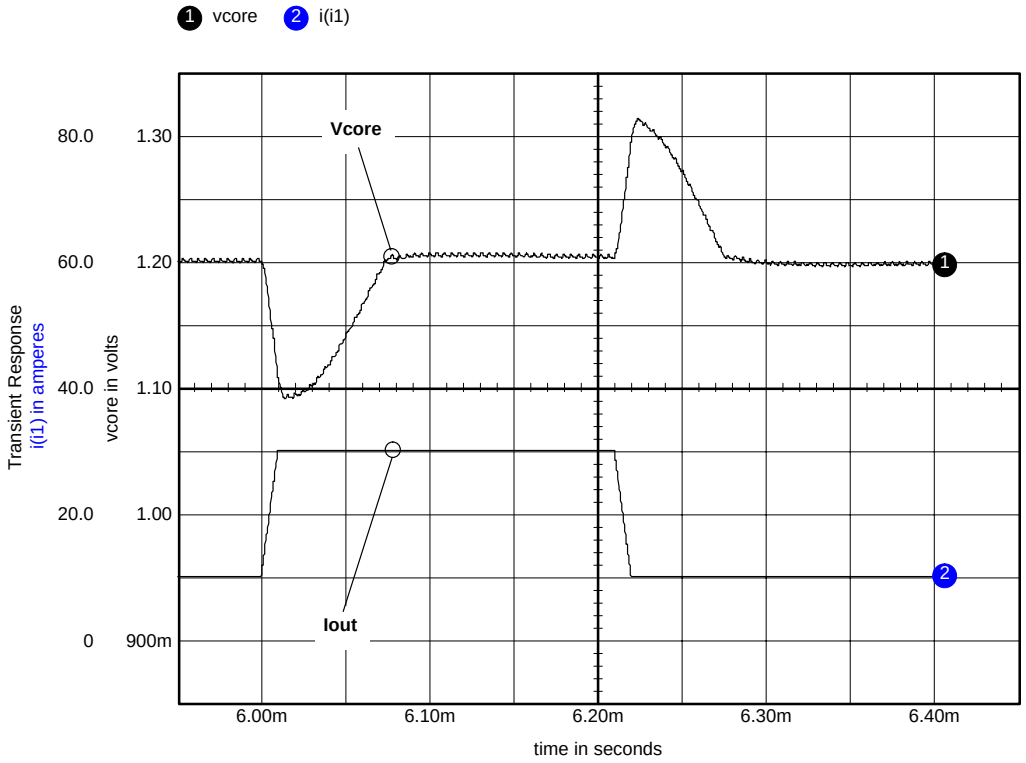


Figure 8. System Transient Response: Io Steps from 10 A to 30 A and Back to 10 A

4. Determine the current sense components and predict the current distribution.

The output inductor is specified to be between 750 nH and 1000 nH. We will use a median value of 875 nH for these calculations. Also, the series resistance of the output inductor (R_L) is specified as 2.5 mΩ.

The NV38 reference design uses current balance resistors of 1.2 K and 1.8 K on the Intersil ISL6569 controller. This forces the phase operating from 5.0 V to conduct 1.8 K/ 1.2 K = 1.5 X more current then the phase operating from 3.3 V. We will use the ratio derived previously that considers the input/output conversion efficiencies: 17.2 A/12.8 A = 1.34.

For this application, we want to accurately balance the phase currents at full load according to a specific ratio. This could be accomplished by two methods. In one method, a resistor divider could be used at the current sense input to reduce the "gain" in that phase which would force more current into that phase. However, the external current signals are usually very low in magnitude (typically less than 20 mV at full load) and reduction of small signals invites noise problems and is not recommended. A better method to steer the currents is to increase the AC signal (external ramp) in one phase to shorten the pulse width and reduce the current in that phase. This is the method that will be used here. Also, the accuracy of the current balance can be improved by increasing the external AC ramp in both phases by using a slightly faster time constant than what is normally selected. Typically, we recommend choosing the current sense components according to $RC = L/R_L$. For this application, we will choose $RC = L/R_L/3$ to improve the accuracy. The drawback to choosing a faster current sense time constant is that the transient response will not be optimal but, luckily, the graphics processor does not demand the same level of transient response as today's Pentium 4 processors.

There are two components of the PWM ramp that must be considered: (1) the external ramp plus DC offset sensed across the output inductor and (2) the fixed internal ramp of the controller at the required duty−cycle. At the PWM comparator, the internal and external signals are combined according to:

$$\mathbf{[I\_avg + G*\Delta I_L/2]*R_L*G_{CSA} + 250\ mV*(Vo/Vi) = COMP}$$

COMP is the steady state voltage from the error amplifier.

I_avg is the average output current of the phase.

ΔI_L is the peak−to−peak current in the output inductor.

R_L is the resistance of the inductor (plus the resistance from the PCB).

250 mV is the magnitude of the NCP5331's internal ramp at 100% duty−cycle.

G_{CSA} is the gain of the current sense amps (specified as 2.1 V/V in the NCP5331 data sheet).

G is the "AC gain" on the external current sense ramp (G = 1 if RC of the sense components is equal to L/R_L).

Substitute the values previously derived in this report to obtain:

$[17.2\ A + G_{5V} * 4.63\ A_{PP}/2] * 2.5\ m\Omega * 2.1\ V/V + 250\ mV * (1.2\ V/5.0\ V) = COMP$, for the 5.0 V phase. (1)

$[12.8\ A + G_{3V} * 3.88\ A_{PP}/2] * 2.5\ m\Omega * 2.1\ V/V + 250\ mV * (1.2\ V/3.3\ V) = COMP$, for the 3.0 V phase. (2)

We must set equations (1) and (2) equal to each other and solve for G_{5V} and G_{3V}. For the best accuracy (see above), we increase the magnitude of the external ramp by setting G_{3V} to 3.0 V/V (to produce three times the normal external ramp) and solve for G_{5V}.

$90.3\ mV + G_{5V}*12.2\ mV + 60\ mV = 97.8\ mV + 90.9\ mV$, solving for G_{5V} results in:

$G_{5V} = 38.4\ mV/12.2\ mV = 3.15\ V/V$

The time constant of the output inductors are L/R_L = 875 nH/2.5mΩ = 350 μs.

The current sense on the 3.3 V phase needs a time constant of 350 μs/3 or 116.7 μs:

$R_{3.3V}C$ = 116.7 μs choose C = 0.01 μF, then $R_{3.3V}$ = 11.7 KΩ (11.8 KΩ is a standard value)

The current sense on the 5.0 V phase needs a time constant of 350 μs/3.15 or 111.1 μs:

$R_{5V}C$ = 111.1 μs choose C = 0.01 μF, then R_{5V} = 11.1 KΩ (11.0 KΩ is a standard value)

An ICAPs (Spice based) simulation of the 2−phase DC/DC converter with the previously derived current sense components was performed to investigate current distribution between the 5.0 V and 3.3 V phases at 1.2 Vout and 30 A load. The RMS output currents from the 5.0 V and 3.3 V phases match the predicted values within 0.1 A at full load as shown in the following graph. The output voltage ripple is less than 5.0 mVpp in this simulation.

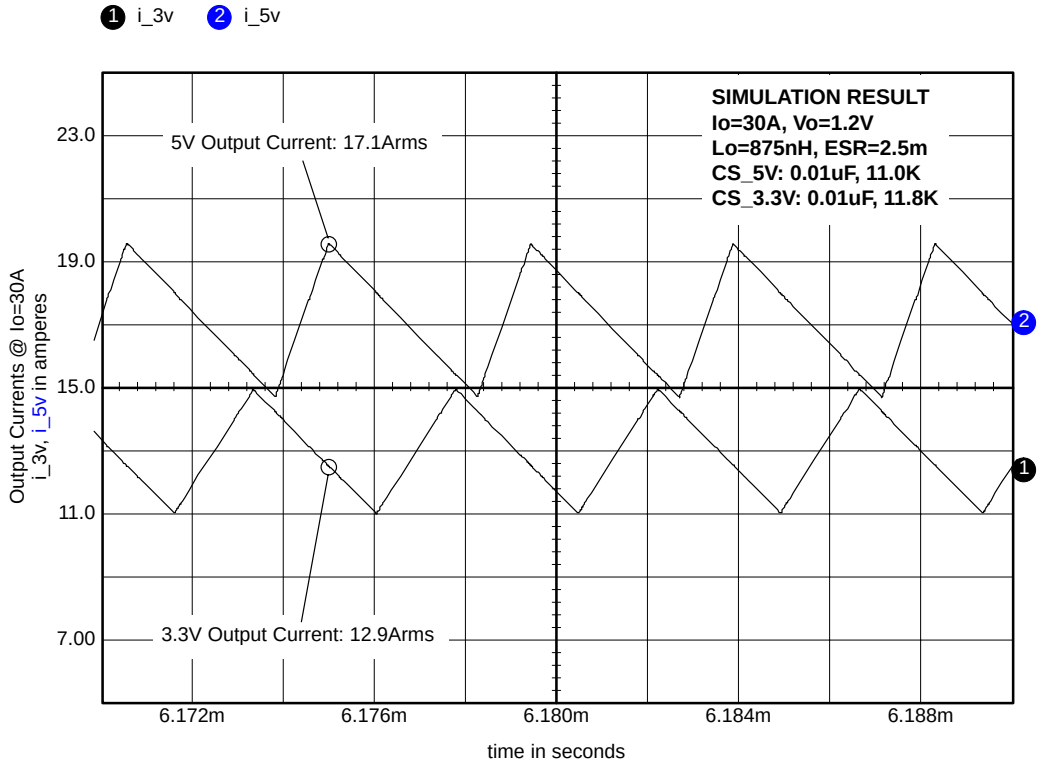


Figure 9.

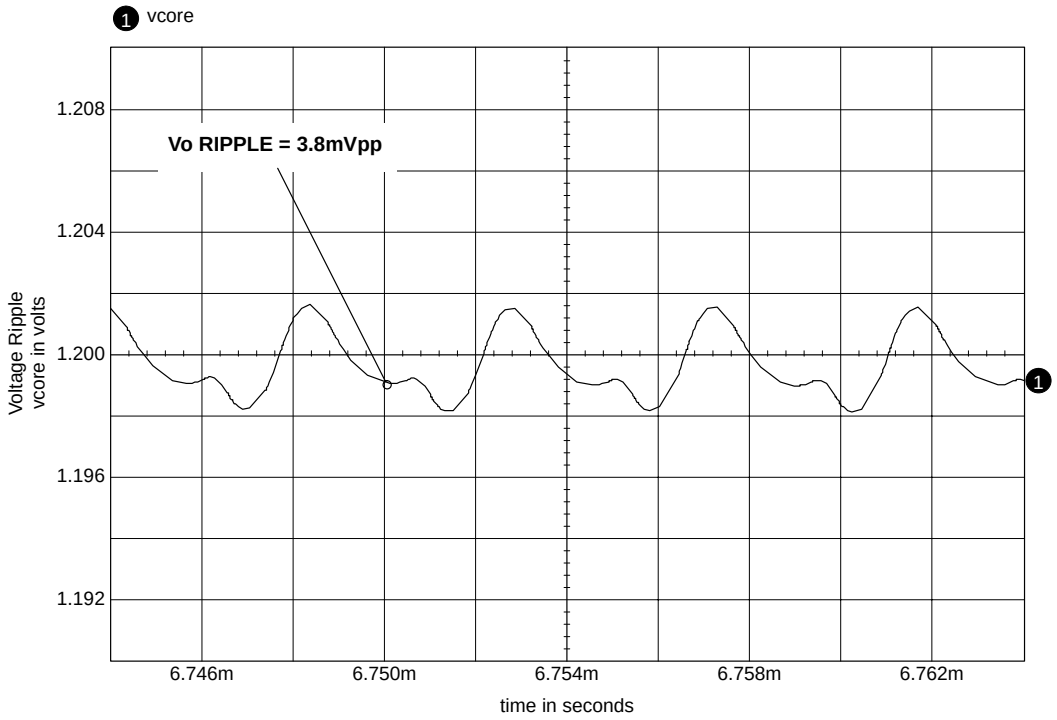


Figure 10.

- Many factors can effect current sharing: PCB layout, inductor saturation, inductor ESR, current sense component tolerances, and PCB resistances. Final current sharing should be carefully examined and fine tuned in the lab on an adequate sample of PCBs. If one phase consistently conducts more (or less) current than desired then the current sensing components may be modified to produce the correct level of current. In general, reducing the current sense resistor (increasing the external ramp) on a phase will reduce the current in that phase. Similarly, increasing the current sense resistor on a phase will increase current in that phase.
- Finally, we must set the over current shutdown threshold. The power section design was performed for 30 A continuous. Considering current ripple, gain tolerances, and inductor ESR change due to temperature rise we choose to set the DC over current shutdown threshold to 48A DC.

  ILIM = (Io_DC + Imax_AC/2) * R_L* G_ILIM +
  = (48 A + 3.0 * 4.63 A_{PP}/2) * 2.5 mΩ * 12 V/V
  = 1.65 Vdc

The voltage divider from the 5.0 VREF pin to the ILIM pin must produce this value. This can easily be done as shown:

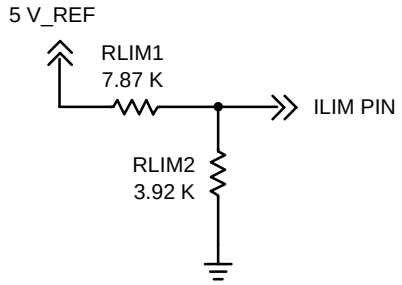


Figure 11.

5. What is the RMS current that the input capacitors must support? How many input capacitors does each phase need?

- Assume the input current has two components: (1) a negative average current when the upper FET is OFF (Iavg) and (2) a peak positive current equal to the converter's maximum output current when the upper FET is ON. Compute the sum of these two RMS currents.
- Assume the converter's efficiency at full load (30 A) will be 80% from the 5.0 V phase and 90% from the 3.3 V phase.

5.0 V Phase	3.3 V Phase
Iavg = Iout * D/Efficiency = 17.2 A * (1.2 V/5.0 V)/0.80 = 5.16 A	Iavg = Iout * D/Efficiency = 12.8 A * (1.2 V/3.3 V)/0.90 = 5.17 A
Irms = $[Iout^2 * D]^{1/2}$ + $[Iavg^2 * (1-D)]^{1/2}$ = 17.2^2 A * (1.2 V/5.0 V)$]^{1/2}$ + $[5.16^2$ A * (1.0−1.2 V/5.0 V)$]^{1/2}$ = 8.42 Arms + 4.49 Arms = 12.91 Arms	Irms = $[Iout^2 * D]^{1/2}$ + $[Iavg^2 * (1-D)]^{1/2}$ = 12.8^2 A * (1.2 V/3.3 V)$]^{1/2}$ + $[5.17^2$ A * (1.0−1.2 V/3.3 V)$]^{1/2}$ = 7.71 Arms + 4.12 Arms = 11.83 Arms

- The capacitors used on the 5.0 V and 3.3 V inputs must support 12.91 Arms and 11.83 Arms over the entire expected temperature range. The Sanyo Oscon series of capacitors is an excellent choice for this application because they offer the highest ripple ratings in the smallest packages. The use of Oscons as input capacitors will be much less expensive then the 3X 100 μF ceramics shown in NVIDIA's reference design.
- It is very important to understand the interaction between the 3.3 V and 5.0 V input currents. At full load, the 5.0 V phase will conduct more current then the 3.3 V phase and both phases will be sourcing current. However, at light loading or no−load operation both phases will not be sourcing current. If the converter loading is less than 5.0 A–7.0 A, then the 5.0 V phase will conduct virtually all of the load current and the 3.3 V phase will probably be sinking current. If the current load on the 3.3 V power supply, due to other components in the system, is extremely low (less than 500 mA) then the "negative" current being delivered by the 3.3 V phase will charge the 3.3 V input capacitors. For this reason, it is recommended that the input capacitors on the 3.3 V phase be rated at 6.3 V and not 4.0 V. The schottky diode D2 shown in the schematic protects the 3.3 V input capacitors by clamping the voltage at approximately 5.6 V. Also, for testing purposes it may be necessary to temporarily populate RL1 and RL2 to load the 3.3 V supply as shown in the Application schematic or the ATX power supply may shut down because of overvoltage due to negative currents from the 3.3 V phase.
- If a thru−hole capacitor is acceptable then Sanyo's SP series can be used:

  5.0 V Phase: 6SP680M (680 μF, 6.3 V, 4.84 Arms, 10.0 mm x 11.5 mm). This phase requires 12.91 Arms/ 4.84 Arms = 2.67 or 3 capacitors on the input for a conservative design.

  3.3 V Phase: 6SP680M (680 μF, 6.3 V, 4.84 Arms, 10.0 mm x 11.5 mm). This phase requires 11.83 Arms/ 4.84 Arms = 2.44 or 3 capacitors on the input for a conservative design.

- If a surface mount capacitor is acceptable then Sanyo's SVP series can be used:

  5.0 V Phase: 6SVP820M (820 μF, 6.3 V, 5.44 Arms, 10.0 mm x 12.7 mm). This phase requires 12.91 Arms/ 5.44 Arms = 2.37 or 3 capacitors on the input for a conservative design.

  3.3 V Phase: 6SVP820M (820 μF, 6.3 V, 5.44 Arms, 10.0 mm x 12.7 mm). This phase requires 11.83 Arms/ 5.44 Arms = 2.17 or 3 capacitors on the input for a conservative design.

- This design was done for a converter with 30 A continuous output. If the actual output current is lower then the number of output capacitors can be reduced.

6. PCB Layout Considerations

a) Place the 1.0 μF ceramic power supply bypass capacitors close to their associated pins: VCCL, VCCH, and VCCL1.

b) Place the MosFETs to minimize the length of the gate traces.

c) Place the components associated with the Error Amplifier to minimize the trace lengths to the pins VFB, VDRP, and COMP.

d) Place the current sense components near the CS1, CS2, and CSREF pins.

e) Place the frequency setting resistor (Rosc) as close as possible to the ROSC pin.

f) The CSREF trace should be routed independently – the remote output voltage sensing trace that connects NVVDD to RFB should not be used as the CSREF connection.

g) A 0.1 μF bypass capacitor should be placed very close to the 5.0 VREF pin (#8).

h) If snubbers are used, they should be placed very close to the lower MosFETs.

i) A 4.7 μF bypass capacitor should be placed very close to each of the upper MosFETs.

j) The signal ground (LGND) should only connect to the ground plane at one point. The LGND connections (shown in the schematic) should be a single point "star" connection to the LGND pin as shown below.

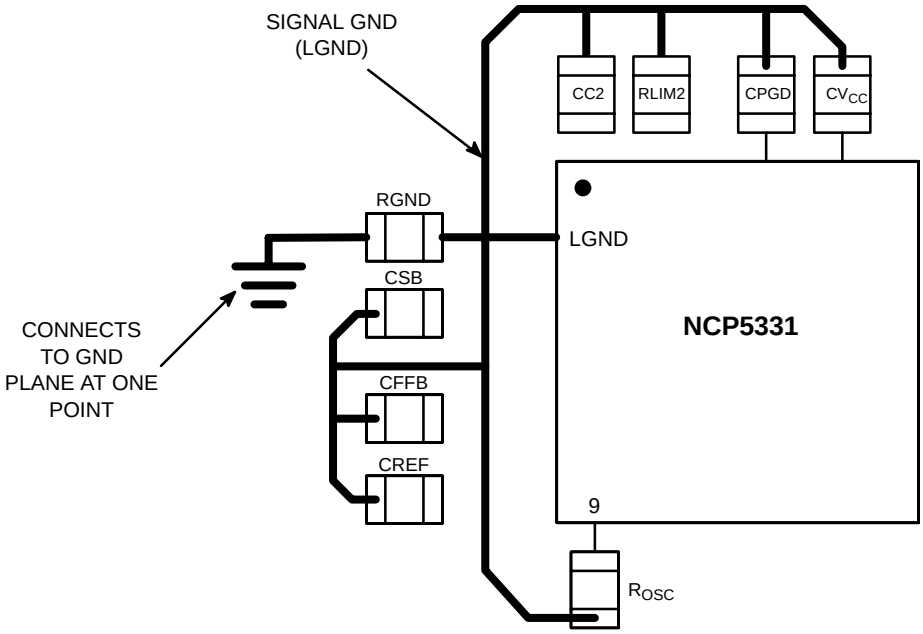


Figure 12.

k) The CSREF connection must be placed between the output inductors or current sharing will not be accurate. The PCB resistance from CSREF to each output inductor should be equal. This is easily accomplished if the output copper is symmetrical around the CSREF sense point as shown below.

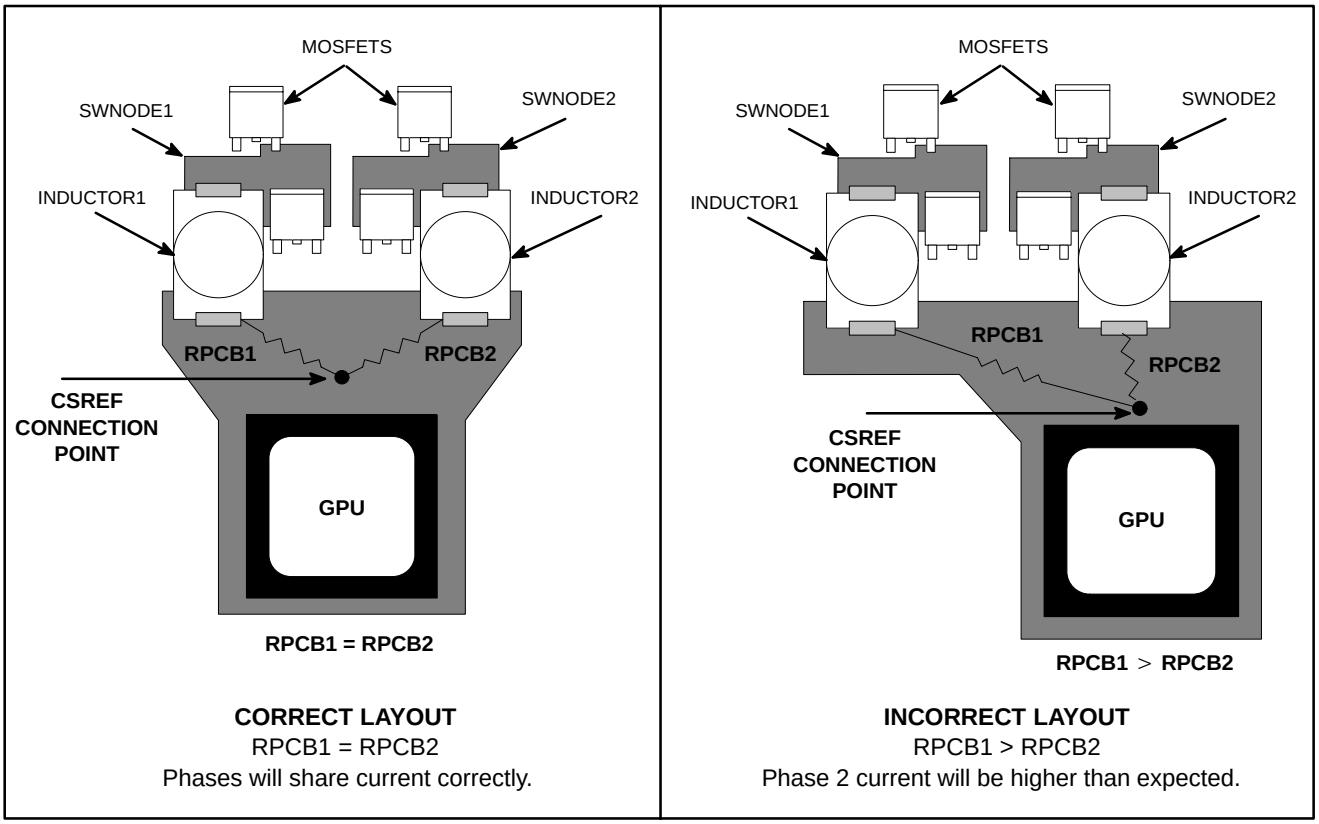


Figure 13.

7. Test Results

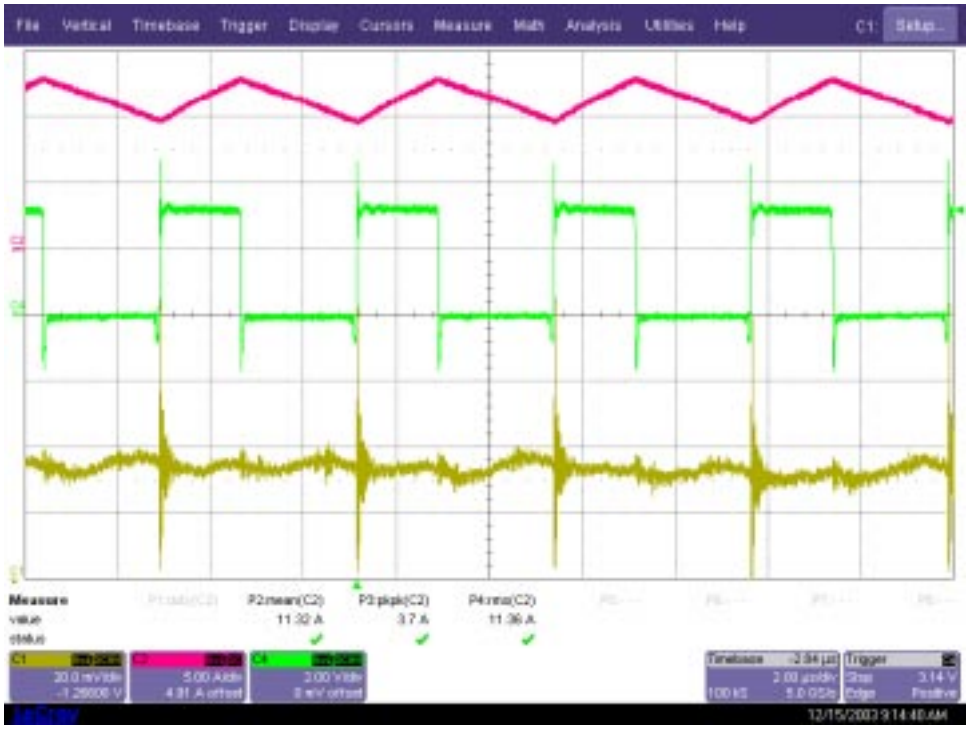
The NCP5331 demo board for AMD's Hammer processor was modified to operate simultaneously from 3.3 V and 5.0 V. The output inductors were modified to produce 825 nH and 2.5 mΩ. The input capacitors were changed to 6.3 V, 680 μF Oscons (three per phase) and the Error Amplifier compensation was changed to the values shown on Page 2 of this report. The output capacitors were changed to a single 820 μF Oscon, 2 x 100 μF ceramics, and 22 x 10 μF ceramics. The current sharing, efficiency, and startup results are shown below.

Table 2. Output Current Sharing vs. Load

I_{out}	I_5.0 V_{out}	I_3.3 V_{out}
(A)	(A)	(A)
0 A	2.21 A	−2.48 A
10 A	8.53 A	1.40 A
20 A	13.6 A	6.48 A
30 A	18.2 A	11.3 A

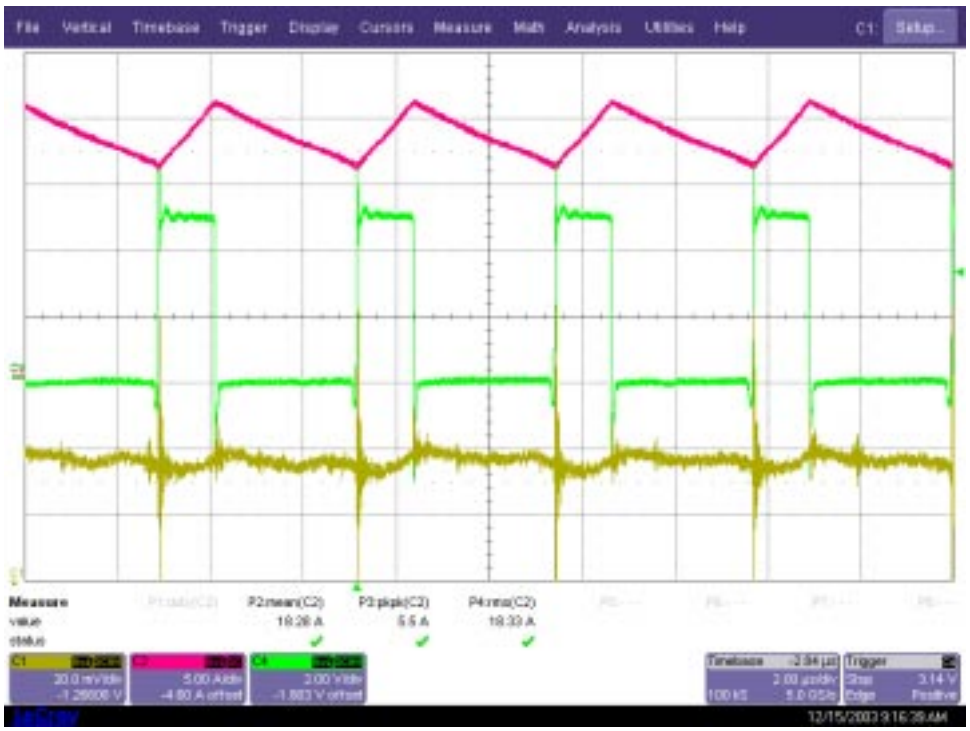
Table 3. Input Currents, Input Voltages, and Efficiencies

V_{out}	I_{out}	5.0 V_{in}	I_5.0 V_{in}	3.3 V_{in}	I_3.3 V_{in}	P_in	P_out	Eff
(V)	(A)	(V)	(A)	(V)	(A)	(W)	(W)	(%)
1.22	5.00	5.07	1.48	3.34	0.24	8.29	6.11	73.73
1.22	10.00	5.04	2.31	3.33	0.52	13.37	12.22	91.37
1.22	15.00	5.02	3.09	3.32	1.48	20.39	18.33	89.92
1.22	20.00	5.00	3.88	3.31	2.58	27.90	24.44	87.61
1.22	25.00	4.98	4.66	3.29	3.72	35.40	30.55	86.30
1.22	30.00	4.95	5.49	3.28	4.98	43.49	36.66	84.30



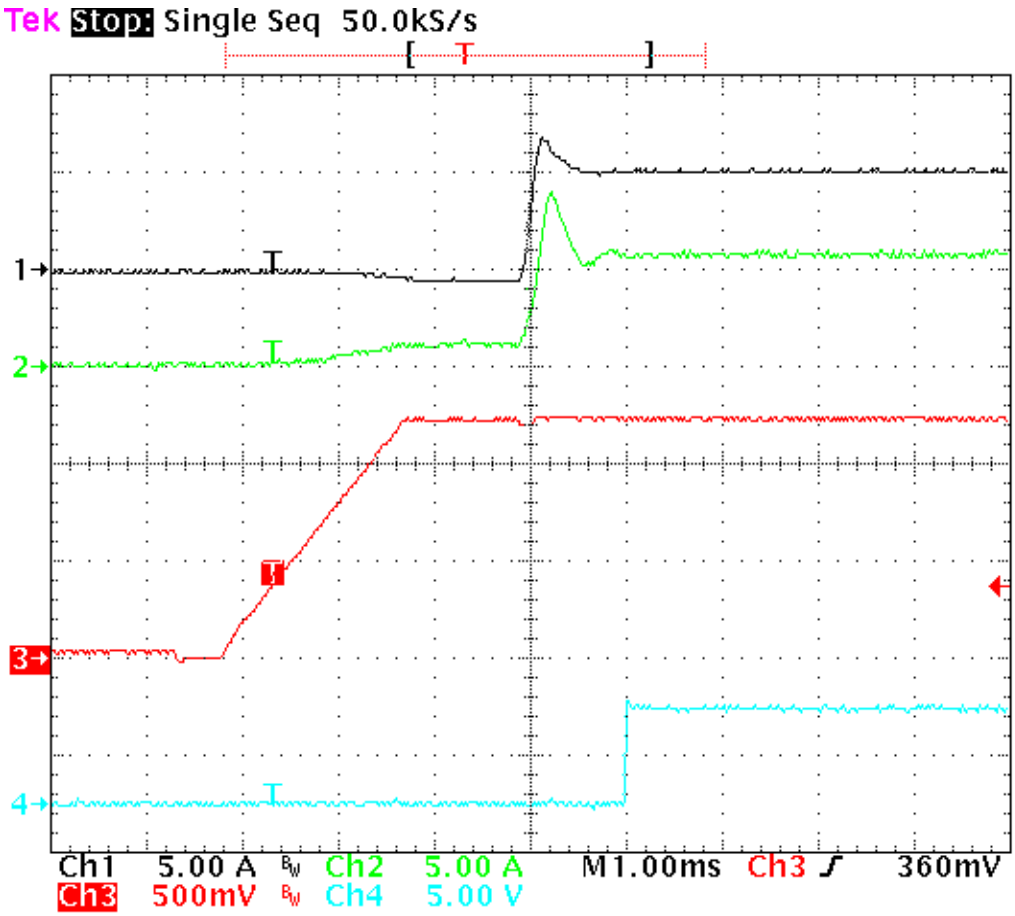
CH1 (20 mV/DIV): Output Voltage (bottom trace)
CH2 (5.0 A/DIV): 3.3 V Output Current at 30 A Load (top trace) – Note the measured average of 11.32 A
CH4 2.0 V/DIV): SWNODE for 3.3 V Phase (middle trace)

Figure 14. 3.3 V Output Current at 30 A Loading



CH1 (20 mV/DIV): Output Voltage (bottom trace)
CH2 (5.0 A/DIV): 5.0 V Output Current at 30 A Load (top trace) – Note the measured average of 18.2 A
CH4 (2.0 V/DIV): SWNODE for 5.0 V Phase (middle trace)

Figure 15. 5.0 V Output Current at 30 A Loading



CH1 (5.0 A/DIV): 3.3 V Input Current (top trace)
CH2 (5.0 A/DIV): 5.0 V Input Current (2nd trace)
CH3 (0.5 V/DIV): Output Voltage (3rd trace)
CH4 (5.0 V/DIV): POWERGOOD (bottom trace)

Figure 16. Startup at 30 A Loading

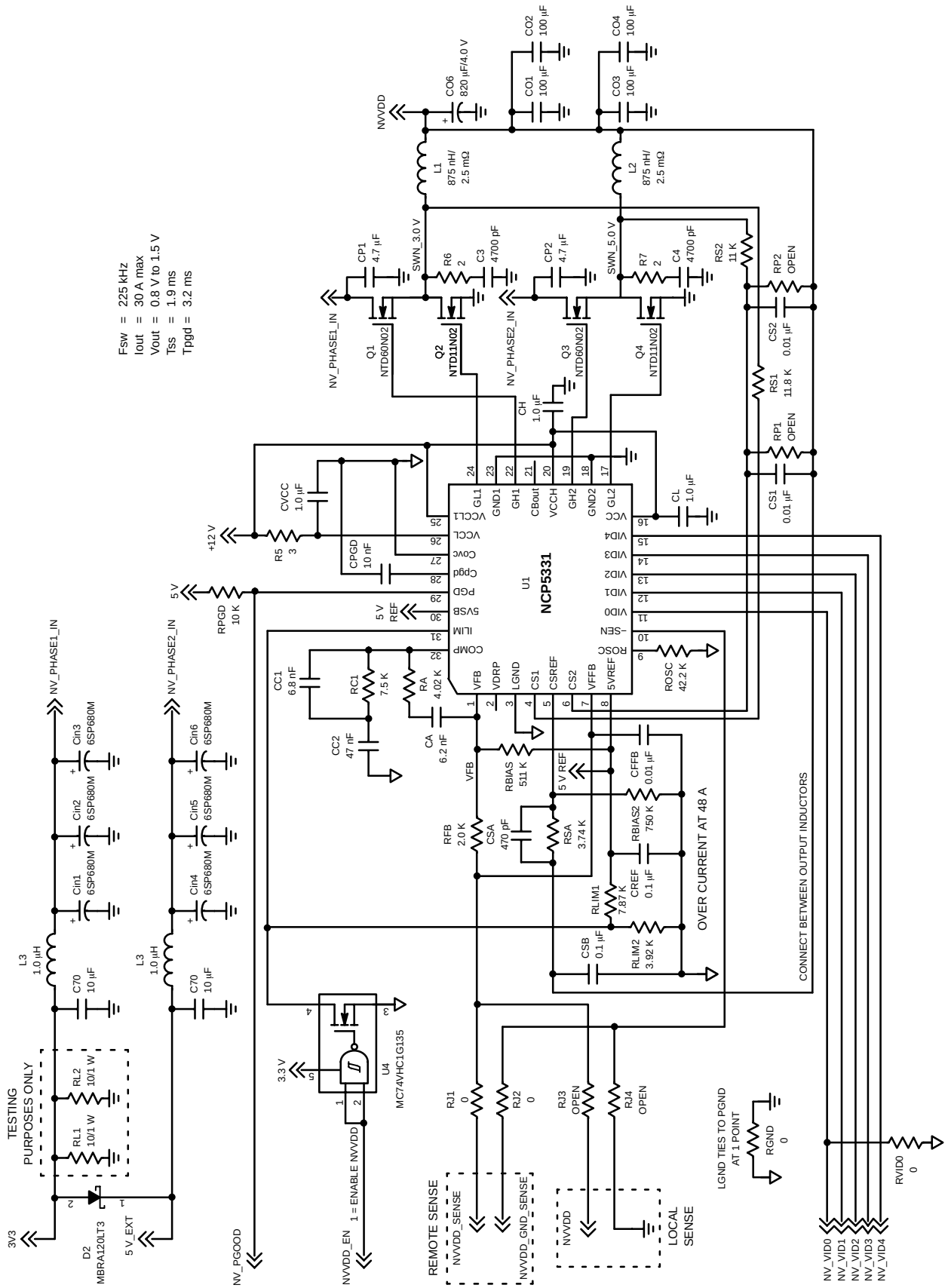


Figure 17. NCP5331 Schematic for NV38 GPU: 0.8 V−1.5 Vo, 30 A, 225 kHz

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